I Claim:

1. A semiconductor chip, comprising:

an active top side;

semiconductor component structures and contact areas disposed on said active top side;

a buffer having a protective layer of a mechanically damping material, said protective layer having a free surface, said buffer:

being disposed between said contact areas and above said semiconductor component structures; and

having a hard coating at said free surface of said protective layer.

2. The semiconductor chip according to claim 1, wherein said buffer has said coating in areas.

3. The semiconductor chip according to claim 1, wherein said coating includes a hard metal selected from one of the group consisting of a chromium-nickel alloy, an oxide ceramic, and a nitride ceramic.

4. The semiconductor chip according to claim 1, wherein said buffer has a substantially circular contour with a diameter of between approximately 50 and approximately 500 μm and a thickness of between approximately 2 and approximately 50 μm.

5. The semiconductor chip according to claim 1, wherein said buffer has a substantially angular contour with a respective side length of between approximately 50 and approximately 500 μm and a thickness of between approximately 2 and approximately 50 μm.

6. The semiconductor chip according to claim 1, wherein:

said active top side has a centroid; and

said buffer is disposed in a region of said centroid.

7. The semiconductor chip according to claim 1, wherein:

said active top side has a centroid; and

said buffer is a plurality of buffer bodies distributed uniformly around a region of said centroid.

8. A semiconductor chip, comprising:

an active top side;

semiconductor component structures and contact areas disposed on said active top side;

a buffer having a protective layer of a mechanically damping material, said protective layer having a free surface, said buffer:

being disposed between said contact areas and above said semiconductor component structures; and

having a mechanically protective coating at said free surface of said protective layer.

9. A semiconductor wafer, comprising:

a plurality of semiconductor chips disposed in rows and columns, each of said semiconductor chips having:

an active top side;

semiconductor component structures and contact areas disposed on said active top side;

a buffer having a protective layer of a mechanically damping material, said protective layer having a free surface, said buffer:

being disposed between said contact areas and above said semiconductor component structures; and

having a hard coating at said free surface of said protective layer.

10. A method for producing a semiconductor wafer, which comprises:

disposing semiconductor component structures and contact areas in rows and columns on an active top side of a semiconductor chip;

providing a buffer with a protective layer of a mechanically damping material and with a protective layer having a hard coating; and

applying the buffer between the contact areas and to the semiconductor component structures.

11. A method for producing a semiconductor wafer, which comprises:

disposing semiconductor component structures and contact areas in rows and columns on an active top side of the semiconductor wafer;

providing a buffer with a protective layer of a mechanically damping material and with a protective layer having a mechanically protective coating; and

applying the buffer between the contact areas and to the semiconductor component structures.

12. A method for producing a semiconductor chip, which comprises:

disposing semiconductor component structures and contact areas on an active top side of the semiconductor chip;

providing a buffer with a protective layer of a mechanically damping material and with a protective layer having a hard coating; and

applying the buffer between the contact areas and above the semiconductor component structures.

13. A method for producing a semiconductor chip, which comprises:

disposing semiconductor component structures and contact areas on an active top side of the semiconductor chip;

providing a buffer with a protective layer of a mechanically damping material and with a protective layer having a mechanically protective coating; and

applying the buffer between the contact areas and above the semiconductor component structures.

14. The method according to claim 10, which further comprises carrying out the application step by:

applying a layer of a mechanically damping material; and

subsequently patterning the damping material layer to form buffer bodies in semiconductor chip positions by one of:

photolithography and etching; and

laser removal.

15. The method according to claim 14, which further comprises providing the damping material layer as a plastic layer.

16. The method according to claim 12, which further comprises carrying out the application step by:

applying a layer of a mechanically damping material; and

subsequently patterning the damping material layer to form buffer bodies in semiconductor chip positions by one of:

photolithography and etching; and

laser removal.

17. The method according to claim 16, which further comprises providing the damping material layer as a plastic layer.

18. The method according to claim 14, which further comprises carrying out the step of applying the buffer bodies in the semiconductor chip positions by printing the damping material layer thereon by one of jet printing technology, screen printing technology, and mask printing technology.

19. The method according to claim 16, which further comprises carrying out the step of applying the buffer bodies in the

semiconductor chip positions by printing the damping material layer thereon by one of jet printing technology, screen printing technology, and mask printing technology.

20. The method according to claim 10, which further comprises carrying out the applying step by applying a multilayer coating to the semiconductor wafer and subsequently patterning the coating to form buffer bodies.

21. The method according to claim 14, which further comprises carrying out the applying step by applying a multilayer coating to the semiconductor wafer and subsequently patterning the coating to form buffer bodies.

22. The method according to claim 18, which further comprises carrying out the applying step by applying a multilayer coating to the semiconductor wafer and subsequently patterning the coating to form buffer bodies.

23. A method for mounting on supports, which comprises:

providing semiconductor chips with active top sides and passive rear sides;

disposing semiconductor component structures and contact areas on the active top sides;

providing a buffer with a protective layer of a mechanically damping material, the protective layer having a free surface, and with a hard coating at the free surface of the protective layer;

disposing the buffer between the contact areas and above the semiconductor component structures;

mounting the semiconductor chips on circuit carriers by:

providing a first transport film with an adhesive top side having a given adhesive strength;

adhesively bonding the semiconductor chips by their passive rear sides on the adhesive top side;

providing a second transport film with an adhesive strength greater than the given adhesive strength;

applying the second transport film to the active top side of the semiconductor chips;

removing the first transport film from the passive rear sides of the semiconductor chips;

supplying the semiconductor chips on the second transport film to a circuit carrier populating device;

successively lifting off the semiconductor chips from the second transport film in the populating device at a lift-off position by at least one piercing tool penetrating through the second transport film and acting on the buffer disposed on the semiconductor chip; and

positioning the semiconductor chips with the semiconductor chip contacts onto corresponding contact pads of the circuit carrier.

24. The method according to claim 23, which further comprises turning the first transport film with the semiconductor chips through 180° before applying the second transport film.

25. The method according to claim 23, which further comprises turning a composite including the first transport film, the second transport film, and the semiconductor chips disposed between the first and second transport films through 180° before removing the first transport film from the passive rear sides of the semiconductor chips.